

SATA PHY PMA Layer IP

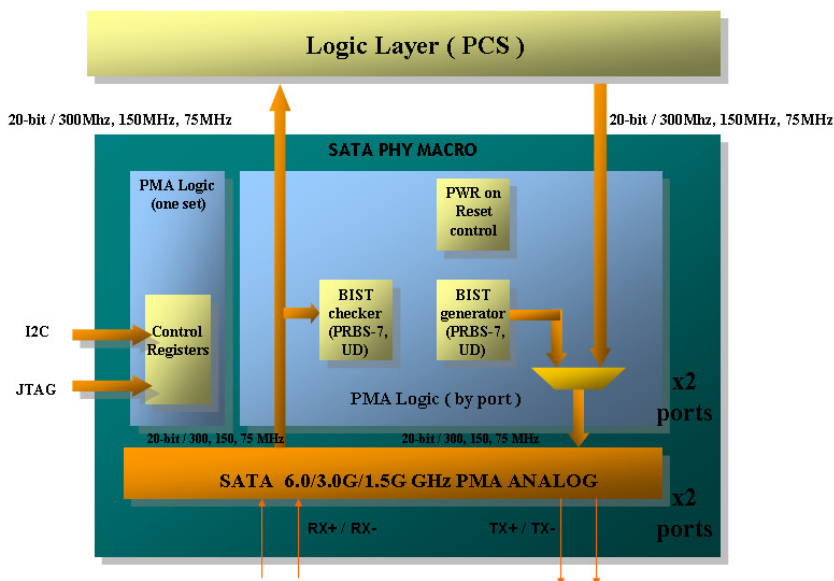
GUC's SATA PHY PMA Layer intellectual property (IP) is designed to conform to the SATA Revision 3.0 Specification. Designed for the latest high-speed backplanes, it supports up to 6 Gbps for high-speed communications and networking applications. Serial ATA (SATA) is the primary internal storage interconnect for desktop and mobile PCs. It connects the host system to peripherals such as hard drives, solid state drives, optical drives, and removable magnetic media devices.

Product Overview

Speed is becoming critical for today's storage solutions, and GUC proves its leadership in this space with its SATA PHY PMA IP designed to comply with Serial ATA Revision 3.0. SATA Revision 3.0 enables 6Gb/s link speeds between storage units, disk drives, optical and tape drives and protocol host bus adaptors (HBAs).

GUC's SATA PHY IP at 6Gb/s promises new levels of performance for networks. It is backward compatible with earlier SATA Implementations of 1.5 and 3Gb/s. GUC's SATA PHY IP maintains the low cost and low power for which SATA is acclaimed.

Based on GUC's proven high-speed SERDES technology, the GUC SATA PHY PMA provides a cost effective and extremely low power solution that is designed to meet the needs of today's high-speed communication and networking designs.



SATA PHY PMA Data Flow

FEATURES AND BENEFITS

SATA PHY PMA Block

- Designed in TSMC 90nm G Process with flip-chip packaging
- Power supply: 1.0V and 1.8V
- Temperature: 0~85C
- Supports SATA 1.5G / 3.0G / 6.0G
- Supports SAS 1.5G / 3.0G / 6.0G
- Supports GUC proprietary PMA interface
- Supports 300MHz / 150MHz / 75MHz frequencies for 20-bit data width mode
- Supports 2 ports
- Supports boundary scan interface for chip global JTAG TAP controller
- Supports user defined JTAG and I2C interfaces for GUC proprietary debug purpose
- Supports IDDQ test mode
- Supports PRBS-7 and User-Defined BIST mode
- Supports individual lane shut down
- Does not support DC coupling for SATA Gen1
- Does not support eSATA
- 6G SAS with 6m to 10 m cable support pending on GUC's test chip silicon results
- Supports symbol alignment and lock COMMA function
- Supports OOB pattern detection function

Test Features

- BIST (built-in-self-test) includes PRBS-7 and user defined 20-bit Pattern
- AC JTAG mode supported for debug
- Supports two loopback modes: serial loopback (PMA loopback) and parallel loopback (PCS loopback)

Process Technology

- TSMC 90nmG 1P7M
- Designed for flip-chip package

SATA PHY PMA Layer IP

SATA PHY PMA IP Deliverables

Item	Description	Format
1	SATA PHY PMA Datasheet	PDF
2	PMA .lib and .db files	.lib / .db
3	PMA behavior simulation model	encrypted VERILOG

Ordering Information

The SATA PHY PMA IP is available as shown below

Part Number	IP Option
IGASATP01A	SATA PHY PMA

NOTE: Consult your GUC sales representative for feature availability and schedule.

Global Unichip IP Products

GUC provides a variety of SerDes IPs including PCIe 1.0/2.0, XAUI PCS and PMA, 1G SerDes PMA, 10G SerDes PMA, SATA 6Gbps PHY PMA, and SAS 6Gbps PMA among others.

GUC offers many valuable IPs for SoC design. For digital IPs, GUC provides USB 1.1/2.0, Ethernet MAC, IDE, JPEG Codec, and TV-encoder products. For Star IPs, GUC carries ARM cores, proprietary DSP, and MPEG-4 Codec. For Analog IPs, GUC offers PLL, POR, ADC, and DAC on different technology nodes. For software IPs, GUC delivers the MP3 codec, AAC-LC Codec, and ARM Codec for audio and speech applications. Additionally, GUC provides SoC integration services from spec to GDSII or RTL to GDSII. GUC is also equipped with the ARM development platform for quick prototyping

GUC's design service covers all fabrication technologies from 0.5μm to 28nm. The high complexity, noise coupling, electro-migration, dynamic IR drop, and design for manufacturing (DFM) problems have now exceeded the capability of traditional design methodology. GUC provides an advanced design flow, which includes quick prototyping, physical synthesis, hierarchical design and clock tree synthesis, static timing analysis, formal verification, power grid design and analysis, cross-talk noise prevention and fixing, on-chip variation (OCV), DFM etc., to achieve rapid timing and signal integrity closure. GUC's design service enables the customer's design to reach power, design-for-testability (DFT), timing and SI closure quickly.

For more information about this product or other Global Unichip services please email us at info@globalunichip.com or visit us on the web at www.globalunichip.com.

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