

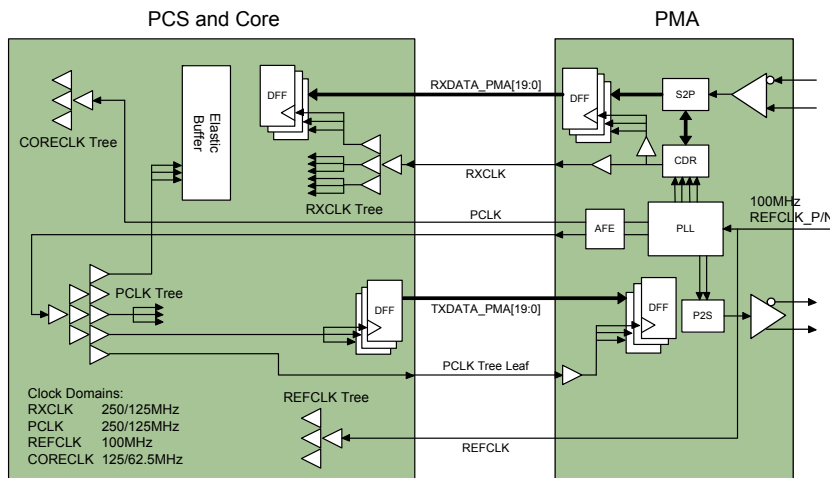
PCI Express 2 Interface PHY Layer IP

GUC's PCIe 2 PHY intellectual property (IP) is designed for use in any networking or high end computing system-on-chip (So-C) solutions. Designed for the latest high-speed backplanes, the PCIe 2 PHY supports the PCI Express 2.0 protocol that is commonly used in high-speed communications applications.

Product Overview

GUC's PCI Express PHY Layer handles the low level PCI Express protocol and signaling. This includes features such as; data serialization and de-serialization, 8b/10b encoding/decoding, analog buffers, elastic buffers and receiver detection. The primary focus of this block is to shift the clock domain of the data from the PCI Express rate to one that is compatible with the general logic in the ASIC.

Based on GUC's proven high-speed SERDES technology, the GUC PCIe 2 PHY provides a cost effective and extremely low power solution that is designed to meet the needs of today's high-speed interconnect designs.



GUC's PCI Express PHY Layer

FEATURES AND BENEFITS

PHY Block

- Supports PIPE 2.0 for PCI Express core logic interface
- Compliant with PCI Express Base Specification Revision 2.0
- Standard PHY interface enables multiple IP sources for PCIe Logical Layer
- Provides target interface for PCI Express PHY vendors
- 250MHz symbol clock for Gen2 speed
- 125MHz symbol clock for Gen1 speed
- Supports 2-symbol design for 16-bit data-width for PIPE interface
- 8b/10b encode and 10b/8b decode
- Symbol lock and symbol alignment
- Supports RX elastic buffer
- Supports TX detect RX protocol
- Supports boundary scan interface for chip global JTAG TAP controller

Physical Media Attachment Layer (PMA)

- Supports GUC's proprietary PCS interface
- Supports PCI Express Base Specification Revision 2.0
- Supports PCI Express Card Electromechanical (CEM) Specification Revision 2.0
- Supports Gen2/Gen1 250MHz/125MHz frequencies for 20-bit data width mode
- Scalable PMA architecture to support X1/X2/X4/X8/X16

Physical Coding Sublayer (PCS)

- Compliant with PIPE 2.0 PCS functions
- Supports PIPE 2.0 for PCS and PCI Express core logic interface
- Supports loopback slave mode with loopback slave FIFO
- Supports PRBS-7 and user defined 40-bit pattern BIST

Test Features

- BIST (built-in-self-test)
- Loopback master and slave modes
- Debug JTAG pin supported for debug
- PMA NAND Tree Test Mode supported
- Boundary Scan Test Mode (implemented in future version)

Adaptable Link/Lane Configurations

- Single-lane, two-lane (X2), and four-lane (X4) configurations
- X8-lane and above configurations use multiple instances of X4-lane PHYs
- Single and multiple link configurations are supported via glue logic.

PCI Express 2 Interface PHY Layer IP

PHY IP Deliverables

Item	Description	Format
1	PCI Express 2.0 PHY Datasheet	PDF
2	PCS RTL source	VERILOG
3	PCS RTL design rule check script and log	Scripts
4	PCS synthesis script	Script
5	PCS formal verification script	Script
6	PMA .db file	.db
7	PMA behavior simulation model	encrypted VERILOG

Ordering Information

The PCIe 2.0 PHY IP is available as shown below

Part Number	IP Option
IGASERS01A IGDPCS001A	PMA hard macro and PCS RTL for PCI Express 2.0 PHY total solution
IGASERS01A	PCI Express 2.0 compliant PMA hard macro

NOTE: Consult your GUC sales representative for feature availability and schedule.

Global Unichip IP Products

GUC provides a variety of SerDes IPs including PCIe 1.0/2.0, XAUI PCS and PMA, 1G SerDes PMA, 10G SerDes PMA, SATA 6Gbps PHY PMA, and SAS 6Gbps PMA among others.

GUC offers many valuable IPs for SoC design. For digital IPs, GUC provides USB 1.1/2.0, Ethernet MAC, IDE, JPEG Codec, and TV-encoder products. For Star IPs, GUC carries ARM cores, proprietary DSP, and MPEG-4 Codec. For Analog IPs, GUC offers PLL, POR, ADC, and DAC on different technology nodes. For software IPs, GUC delivers the MP3 codec, AAC-LC Codec, and ARM Codec for audio and speech applications. Additionally, GUC provides SoC integration services from spec to GDSII or RTL to GDSII. GUC is also equipped with the ARM development platform for quick prototyping

GUC's design service covers all fabrication technologies from 0.5 μ m to 28nm. The high complexity, noise coupling, electro-migration, dynamic IR drop, and design for manufacturing (DFM) problems have now exceeded the capability of traditional design methodology. GUC provides an advanced design flow, which includes quick prototyping, physical synthesis, hierarchical design and clock tree synthesis, static timing analysis, formal verification, power grid design and analysis, cross-talk noise prevention and fixing, on-chip variation (OCV), DFM etc., to achieve rapid timing and signal integrity closure. GUC's design service enables the customer's design to reach power, design-for-testability (DFT), timing and SI closure quickly.

For more information about this product or other Global Unichip services please email us at info@globalunichip.com or visit us on the web at www.globalunichip.com

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