

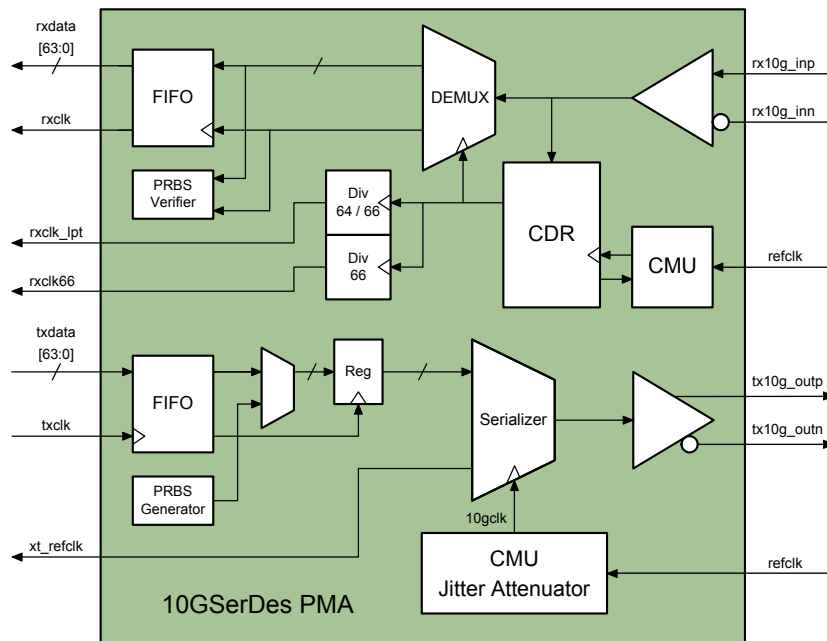
## 10G SerDes PMA Layer IP

GUC's 10G SerDes PMA Layer intellectual property (IP) is designed to meet multiple standards in XFI and CEI-11G. It can support 10G EPON applications as well as networking or high end computing system-on-chip (So-C) solutions. Designed for the latest high-speed backplanes, this 10G SerDes PMA supports from 9.95Gb/s up to 12.5Gb/s for high-speed communications and networking applications.

### Product Overview

Over the last several years designers have been challenged to obtain higher data rates, reduce PCB traces, reduce connectors, and reduce EMI emissions and susceptibility. SERDES technologies have become increasingly popular as a method to meet these challenges for chip-to-chip and backplane applications.

Based on GUC's proven high-speed SERDES technology, the GUC 10G SerDes PMA provides a cost effective and extremely low power solution that is designed to meet the needs of today's high-speed communication and networking designs.



GUC's 10G SerDes PMA Layer

### FEATURES AND BENEFITS

#### 10G SerDes PMA Block

- Supports XFI and CEI-11G standards
- Supports 10G EPON application
- Supports standard 9.95Gb/s and up to 12.5Gb/s data rates
- Bist options supported
- Supports digital Loss of Lock (LoL)
- Supports digital Loss of Signal (LoS)
- TX equalization with de-emphasis range from 0dB to -9.5dB
- RX equalization implementation
- TX supports both AC and DC coupling, RX supports AC coupling only
- RX automatic/manual threshold adjust implementation to achieve extremely high RX sensitivity
- 64b/66b encode and 64b/66b decode
- Supports I2C ports for configuration registers access and test mode control
- Supports AHB/Serial interface for register configuration and test mode control

#### Test Features

- BIST (built-in-self-test) includes PRBS-7, PRBS-31 and user defined 64-bit pattern generator and verifier
- AC JTAG mode supported for debug
- Supports two loopback modes: serial loopback (PMA loopback) and parallel loopback (XSBI loopback)

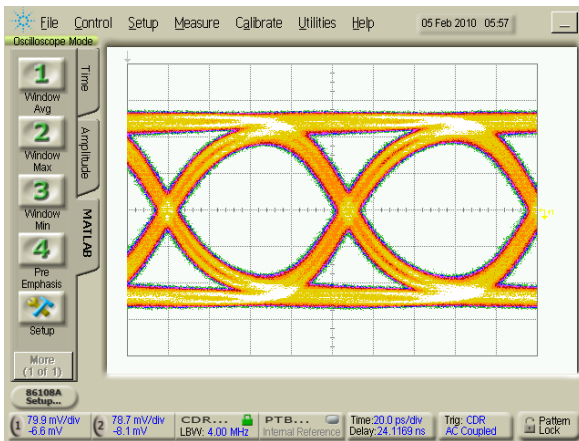
#### Process Technology

- TSMC 40nmG 7M/8M
- Low  $V_t$  devices
- Deep N-well
- Designed for flip-chip package

## 10G SerDes PMA Layer IP

### High Performance TX Transmitter

The figure below shows the output of the TX transmitter.



PRBS31 Data at 11Gb/s

### 10G SerDes PMA IP Deliverables

Item	Description	Format
1	10G SerDes PMA Datasheet	PDF
2	PCS RTL source	VERILOG
3	PCS RTL design rule check script and log	Scripts
4	PCS synthesis script	Script
5	PCS formal verification script	Script
6	PMA .lib and .db files	.lib / .db
7	PMA behavior simulation model	encrypted VERILOG

### Ordering Information

The 10G SerDes PMA IP is available as shown below

Part Number	IP Option
IGASERS02A	10G SerDes PMA

NOTE: Consult your GUC sales representative for feature availability and schedule.

### Global Unichip IP Products

GUC provides a variety of SerDes IPs including PCIe 1.0/2.0, XAUI PCS and PMA, 1G SerDes PMA, 10G SerDes PMA, SATA 6Gbps PHY PMA, and SAS 6Gbps PMA among others.

GUC offers many valuable IPs for SoC design. For digital IPs, GUC provides USB 1.1/2.0, Ethernet MAC, IDE, JPEG Codec, and TV-encoder products. For Star IPs, GUC carries ARM cores, proprietary DSP, and MPEG-4 Codec. For Analog IPs, GUC offers PLL, POR, ADC, and DAC on different technology nodes. For software IPs, GUC delivers the MP3 codec, AAC-LC Codec, and ARM Codec for audio and speech applications. Additionally, GUC provides SoC integration services from spec to GDSII or RTL to GDSII. GUC is also equipped with the ARM development platform for quick prototyping

GUC's design service covers all fabrication technologies from 0.5 $\mu$ m to 28nm. The high complexity, noise coupling, electro-migration, dynamic IR drop, and design for manufacturing (DFM) problems have now exceeded the capability of traditional design methodology. GUC provides an advanced design flow, which includes quick prototyping, physical synthesis, hierarchical design and clock tree synthesis, static timing analysis, formal verification, power grid design and analysis, cross-talk noise prevention and fixing, on-chip variation (OCV), DFM etc., to achieve rapid timing and signal integrity closure. GUC's design service enables the customer's design to reach power, design-for-testability (DFT), timing and SI closure quickly.

### Contact Us

#### Global Unichip (Headquarters)

No. 10, Li-Hsin 6th Road  
 Hsinchu Science Park  
 Hsinchu, Taiwan, R.O.C.  
 Tel: 886-3-5646600  
 Fax: 886-3-5646000

#### Global Unichip (China)

1806 Hong Yi Plaza  
 No. 288 Jiu Jiang Road  
 Huangpu District  
 Shanghai, China 200001  
 Tel: 86-21-3366-5868  
 Fax: 86-21-3366-5878

#### Global Unichip (Korea)

15F, AnnJay Tower, 718-2  
 Yeoksam-dong, Gangnam-gu  
 Seoul 135-080, Korea  
 Tel: 82-2-553-3842  
 Fax: 82-2-553-3846

#### Global Unichip (Japan)

Yokohama Landmark Tower 16F  
 2-2-1, Minatomirai, Nishiku  
 Yokohama, 220-8116, Japan  
 Tel: 81-45-222-8256  
 Fax: 81-45-222-8259

#### Global Unichip (Europe B.V.)

World Trade Center  
 Zuidplein 60 1077XV  
 Amsterdam  
 Tel: 31-20-7184888  
 Fax: 31-20-7184889

#### Global Unichip (USA)

2700 Zanker Road #168  
 San Jose, CA 95134  
 Tel: 408-382-8901  
 Fax: 408-321-8299

<http://www.globalunichip.com>  
 Email: [info@globalunichip.com](mailto:info@globalunichip.com)