

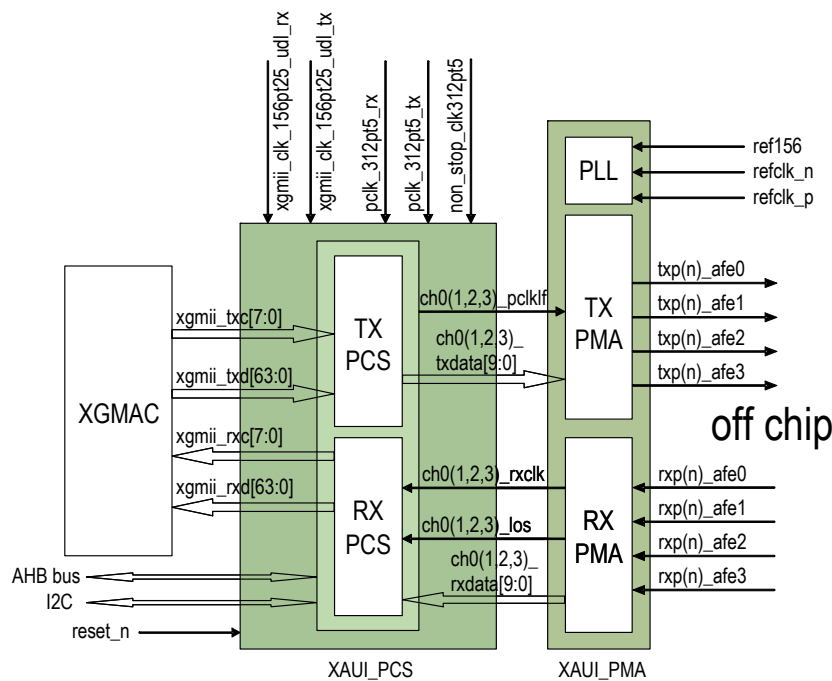
## XAUI PHY Layer IP

GUC's 10 Gigabit Attachment Unit Interface (XAUI) PHY intellectual property (IP) is designed for use in any networking or high end computing system-on-chip (So-C) solutions. Designed for the latest high-speed backplanes, the XAUI PHY supports the 10 Gigabit Ethernet protocols that are commonly used in high-speed communications applications.

### Product Overview

The XAUI standard was designed to accommodate increasing communication systems speeds by dividing a 10 Gbps data stream into four lanes conveying the 8b/10b encoded data and control at 3.125Gbps. These four serial streams are designed to run over copper traces and chip-to-chip connections to deliver high performance communication.

Based on GUC's proven high-speed SERDES technology, the GUC XAUI PHY provides a cost effective and extremely low power solution that is designed to meet the needs of today's XAUI designs.



GUC's XAUI PHY Layer

### FEATURES AND BENEFITS

#### XAUI PHY Block

- Supports IEEE 802.3ae clause 47, 48 standards
- Supports IEEE 802.3az Draft v2.1 feature
- XAUI low-swing AC coupled differential interface
- Supports 10-bit data width under a 312.5MHz digital parallel interface
- The signal paths are intended to operate up to 50cm over controlled impedance traces on standard FR4 printed circuit boards
- 8b/10b encode and 10b/8b decode
- Supports I2C ports for configuration registers access and test mode control
- Supports AHB/Serial interface for register configuration and test mode control
- Supports RX elastic buffer
- Supports TX detect RX protocol

#### Physical Media Attachment Layer (PMA)

- Supports GUC's proprietary PCS interface
- Supports power-on sequence control
- Supports 4-lane design
- Supports serial and parallel loopback modes
- Supports loss of lock
- Designed in TSMC 40nm general logic process
- Uses 7 layers of metal
- Designed for flip-chip packaging

#### Physical Coding Sublayer (PCS)

- XAUI PCS function compliant with IEEE 802.3ae Clause 47, 48 specification
- Four channels with 3.125Gbps per channel providing 10-Gbps data throughput
- 10-bits per lane, four lane interface for transmit and receive path with XAUI PMA
- 64-bit XGMII interfaces easily connected to 10 Gigabit Ethernet MAC core
- Implements XGXS independent transmit and receive data paths
- Utilization of 8b/10b coding
- Supports jumbo Ethernet packet up to 16Kbytes
- Supports loopback slave mode with loopback slave FIFO

#### Test Features

- BIST (built-in-self-test) includes PRBS-7, PRBS-31 and user defined 40-bit Pattern
- Near-end loopback before 8b/10b encoder/decoder, far-end loopback after 8b/10b encoder/decoder

## XAUI PHY Layer IP

### PHY IP Deliverables

Item	Description	Format
1	XAUI PHY Datasheet	PDF
2	PCS RTL source	VERILOG
3	PCS RTL design rule check script and log	Scripts
4	PCS synthesis script	Script
5	PCS formal verification script	Script
6	PMA .db file	.db
7	PMA behavior simulation model	encrypted VERILOG

### Ordering Information

The XAUI PHY IP is available as shown below

Part Number	IP Option
IGASERS05A	XAUI PHY IP

NOTE: Consult your GUC sales representative for feature availability and schedule.

### Global Unichip IP Products

GUC provides a variety of SerDes IPs including PCIe 1.0/2.0, XAUI PCS and PMA, 1G SerDes PMA, 10G SerDes PMA, SATA 6Gbps PHY PMA, and SAS 6Gbps PMA among others.

GUC offers many valuable IPs for SoC design. For digital IPs, GUC provides USB 1.1/2.0, Ethernet MAC, IDE, JPEG Codec, and TV-encoder products. For Star IPs, GUC carries ARM cores, proprietary DSP, and MPEG-4 Codec. For Analog IPs, GUC offers PLL, POR, ADC, and DAC on different technology nodes. For software IPs, GUC delivers the MP3 codec, AAC-LC Codec, and ARM Codec for audio and speech applications. Additionally, GUC provides SoC integration services from spec to GDSII or RTL to GDSII. GUC is also equipped with the ARM development platform for quick prototyping

GUC's design service covers all fabrication technologies from 0.5 $\mu$ m to 28nm. The high complexity, noise coupling, electro-migration, dynamic IR drop, and design for manufacturing (DFM) problems have now exceeded the capability of traditional design methodology. GUC provides an advanced design flow, which includes quick prototyping, physical synthesis, hierarchical design and clock tree synthesis, static timing analysis, formal verification, power grid design and analysis, cross-talk noise prevention and fixing, on-chip variation (OCV), DFM etc., to achieve rapid timing and signal integrity closure. GUC's design service enables the customer's design to reach power, design-for-testability (DFT), timing and SI closure quickly.

For more information about this product or other Global Unichip services please email us at [info@globalunichip.com](mailto:info@globalunichip.com) or visit us on the web at [www.globalunichip.com](http://www.globalunichip.com).

### Contact Us

#### Global Unichip (Headquarters)

No. 10, Li-Hsin 6th Road  
 Hsinchu Science Park  
 Hsinchu, Taiwan, R.O.C.  
 Tel: 886-3-5646600  
 Fax: 886-3-5646000

#### Global Unichip (China)

1806 Hong Yi Plaza  
 No. 288 Jiu Jiang Road  
 Huangpu District  
 Shanghai, China 200001  
 Tel: 86-21-3366-5868  
 Fax: 86-21-3366-5878

#### Global Unichip (Korea)

15F, AnnJay Tower, 718-2  
 Yeoksam-dong, Gangnam-gu  
 Seoul 135-080, Korea  
 Tel: 82-2-553-3842  
 Fax: 82-2-553-3846

#### Global Unichip (Japan)

Yokohama Landmark Tower 16F  
 2-2-1, Minatomirai, Nishiku  
 Yokohama, 220-8116, Japan  
 Tel: 81-45-222-8256  
 Fax: 81-45-222-8259

#### Global Unichip (Europe B.V.)

World Trade Center  
 Zuidplein 60 1077XV  
 Amsterdam  
 Tel: 31-20-7184888  
 Fax: 31-20-7184889

#### Global Unichip (USA)

2700 Zanker Road #168  
 San Jose, CA 95134  
 Tel: 408-382-8901  
 Fax: 408-321-8299

<http://www.globalunichip.com>  
 Email: [info@globalunichip.com](mailto:info@globalunichip.com)