

UADC-8012A-180MS

0.18 μ m MS 3.3V/1.8V 12-bit 1Msps SAR ADC [8ch]

Features

- ◆ 0.18 μ m 1.8V/3.3V mixed-signal CMOS process with 1P5M layout
- ◆ 12-bit resolution
- ◆ 1Msps conversion rate
- ◆ Dual supply voltage (3.3V for analog; 1.8V for digital)
- ◆ 8 input channels
- ◆ Single-end input available (0V~2V)
- ◆ Monotonic guaranteed
- ◆ Power down mode available
- ◆ Power dissipation : 2mW
- ◆ Operation temperature range:0 $^{\circ}$ C~85 $^{\circ}$ C
- ◆ Core cell area : 0.19 mm²
- ◆ Test chip available in LQFP-64 package

Applications

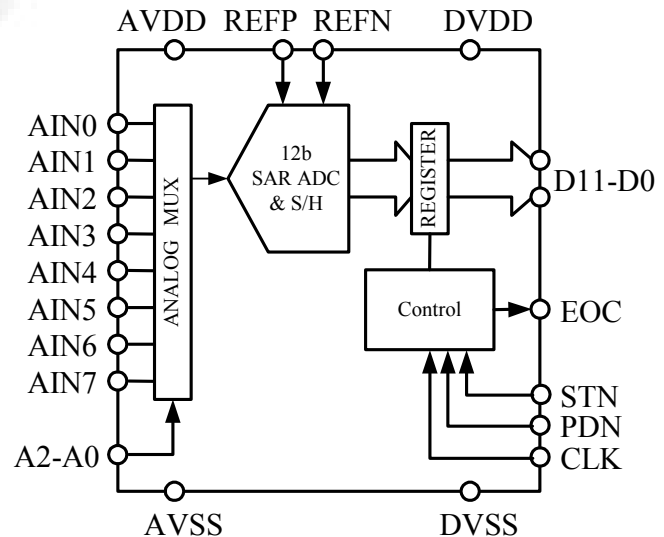
- Hardware monitoring or fan speed control
- Battery voltage detection
- Voice recording
- Microprocessor peripheral

Overview

UADC-8012A-180MS is a general-purpose analog to digital converter (ADC) with 8 multiplexed analog input channels. The architecture of ADC is successive approximation register (SAR) type. The reference voltage and clock signal are controlled external.

A power down mode is available to disable the ADC. It is used for lower power dissipation in standby mode.

Block Diagram



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Description

The UADC-8012A-180MS is a 12-bit analog to digital converter with throughput of 1M samples per second. The analog input voltage was compared to external reference voltages REFP and REFN, and then converted to unsigned binary digital code. The input full swing of ADC is defined by reference voltages REFP and REFN, normally 0V~2V.

Deliverables

- Comprehensive document set
- Hard macro
- Synopsys™ synthesis model
- Verilog model
- TLF model
- LEF model
- Testchip and evaluation board

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