

UAPC-1200 Vectored Interrupt Controller

Features

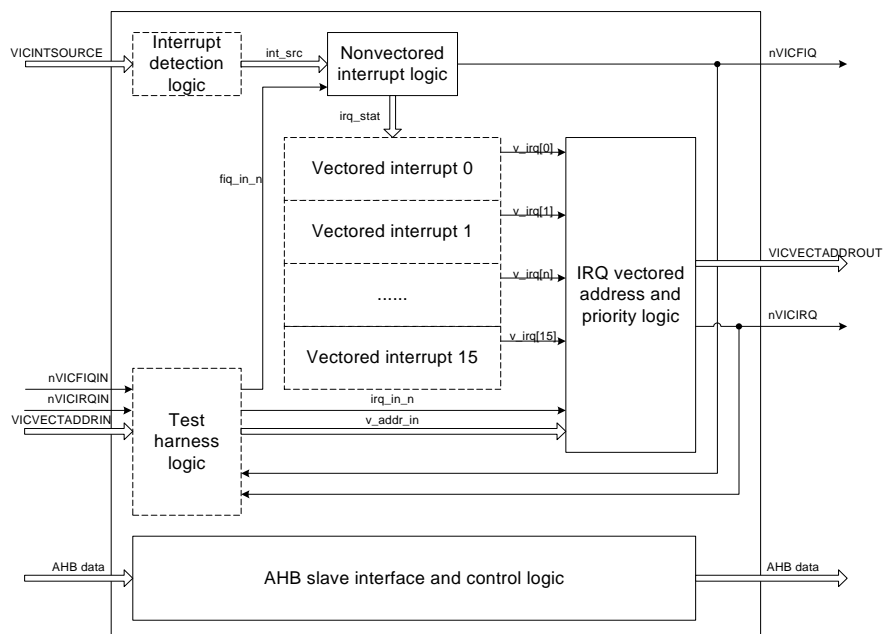
- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Support for 16 or 32 standard interrupts
- ◆ Support for 8 or 16 vectored IRQ interrupts
- ◆ Hardware interrupts priority
- ◆ IRQ and FIQ generation
- ◆ AHB mapped for faster interrupt response
- ◆ Software interrupt generation
- ◆ Provide test registers
- ◆ Raw interrupt status
- ◆ Interrupt request status
- ◆ Interrupt masking
- ◆ Privileged mode support
- ◆ Vector interrupt controller daisy chaining support
- ◆ Provide programmable interrupt source type

Overview

The UAPC-1200 is a synthesizable soft IP core connected to AMBA™ AHB bus for easy integration into SOC implementations.

The UAPC-1200 has 16 or 32 interrupt lines. It uses a bit position for each different interrupt source. It generates IRQ and FIQ for ARM processor. The software can control each request line to generate software interrupts. There are 8 or 16 vectored interrupts. The vectored and nonvectored IRQ interrupts provide an address for an Interrupt Service Routine (ISR).

Block Diagram



Global Unichip Corp.

TEL: +886-3-5646600 <http://www.globalunichip.com>
 FAX: +886-3-5646000 e-mail: info@globalunichip.com
 No. 10, Li-Hsin 6th Rd., Hsinchu Science Park, Hsinchu 300, Taiwan

Description

The UAPC-1200 is a vectored interrupt controller for ARM processor. It is an AMBA™ compliant SOC peripheral. It is a slave module that connects to the AHB bus. It provides a software interface to the interrupt system.

The UAPC-1200 has 16 or 32 interrupt lines. It generates IRQ and FIQ for ARM processor. It uses a bit position for each different interrupt source. The software can control each request line to generate software interrupts. There are 8 or 16 vectored interrupts. The vectored and nonvectored IRQ interrupts provide an address for an Interrupt Service Routine (ISR).

The FIQ interrupt has the highest priority, followed by interrupt vector 0 to interrupt vector 7 or 15. Nonvectored IRQ interrupts have the lowest priority. A programmed interrupt request generates an interrupt under software control. This register is typically used to downgrade an FIQ interrupt to an IRQ interrupt. The UAPC-1200 can daisy-chain a second UAPC-1200 controller for more interrupt lines.

The UAPC-1200 provides the programmable interrupt detector to detect several interrupt source type: rising, falling, or both edge triggered; or high or low level sensitive.

Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

Global Unichip Corp.

TEL: +886-3-5646600 <http://www.globalunichip.com>
FAX: +886-3-5646000 e-mail: info@globalunichip.com
No. 10, Li-Hsin 6th Rd., Hsinchu Science Park, Hsinchu 300, Taiwan