

## UAPC-1500 Watchdog Timer

### Features

- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Provide 3 sets of independent signals to indicate time out.
- ◆ 32-bits counter

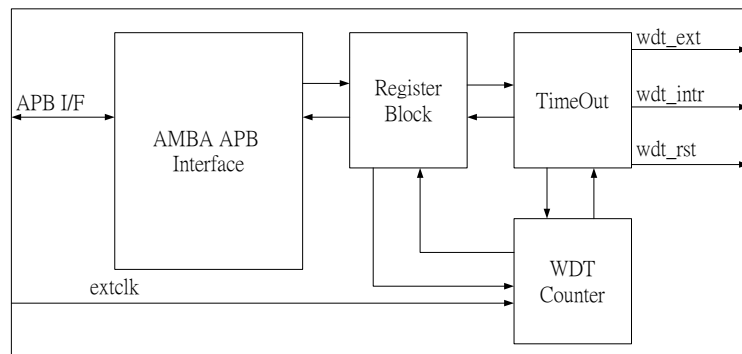
### Overview

The UAPC-1500 *Watchdog Timer* (WDT) is an *Advanced Microcontroller Bus Architecture* (AMBA) compliant System-on-Chip (SOC) peripheral that is developed, tested and licensed by GUC.

The GUC WDT is an AMBA slave module that connects to the *Advanced Peripheral Bus* (APB).

The GUC WDT protects against system failures by providing a method of escaping from unexpected events or programming errors. One activated, the timer must be serviced by software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the watchdog timer module either asserts a system reset signal, or an interrupt request signal. Depending on software configuration

### Block Diagram



### Description

GUC WDT comprises:

- An AMBA APB interface.
- Counter
- Programmable period register

The CPU reads and writes data and control/status information via the AMBA APB interface.

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One counter is decremented on successive rising edges of the input clock extclk or apb\_clk. If the GUC WDT counter reaches zero, time-out condition occur, then wdt\_rst, wdt\_intr or wdt\_ext signal will be asserted and keep on certainly cycle time. Those signals can read from status register and it is clear by writing 1(one) to clear register.

Before WDT timer time out, user can reload counter value by control reload register, that will lead to WDT timer value be reset to reload value. And restart down count.

### **Deliverables**

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

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