

UAPC-1600 TIMER

Features

- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Programmable 32-bit timer/counters
- ◆ Up to three (3) set of independent timer/counters
- ◆ Interrupt generated either overflow or regular intervals
- ◆ Two match registers
- ◆ Current value of each count register can be read at any time

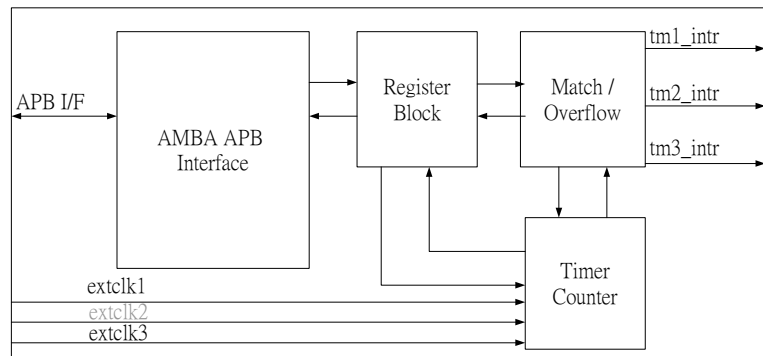
Overview

The UAPC-1600 TIMER is an *Advanced Microcontroller Bus Architecture* (AMBA) compliant System-on-Chip (SOC) peripheral that is developed, tested and licensed by GUC.

The GUC TIMER is an AMBA slave module that connects to the *Advanced Peripheral Bus* (APB).

The GUC TIMER can be used to provide a match function or counters. This is achieved by generating interrupt signals after counter underflow or meet match register.

Block Diagram



Description

GUC TIMER comprises:

- An AMBA APB interface.
- A 32-bit counter
- Two 32-bit match register
- Two 32-bit comparator

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The CPU reads and writes data and control/status information via the AMBA APB interface.

The 32-bit counter is decremented on successive rising edges of the input clock `tmn_clk` or `pclk`. The counter is loaded with a start value by write to the load register. The value of the counter may be obtained at any time by read the counter status register. When the counter reach the zero value, it wraps to load value and continues decrementing.

The match register is programmed by writing to match register. The counter and match values are compared in a comparator. When both values are equal, the interrupt is asserted HIGH. The CPU can use the interrupt to implement a basic time function. The value in the match register may be read at any time.

Writing to the interrupt control register can mask the interrupt signals. The status of the interrupt may be obtained by reading status register.

Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

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