

UAPC-2300 I²C Interface

Features

- ◆ Compliance with the AMBA Specification 2.0 and the SFR interface of 8051
- ◆ Software programmable clock frequency setting for I²C master
- ◆ Software programmable acknowledgement bit
- ◆ Software programmable slave address setting for I²C slave
- ◆ I²C Master can operate as either master-transmitter or master-receiver
- ◆ I²C Slave can operate either slave-transmitter or slave-receiver
- ◆ Interrupt driven data transfer
- ◆ Start / Stop / Repeated Start / Acknowledge generation
- ◆ Support Clock Stretching / Wait state generation
- ◆ Single Master Operation
- ◆ Operational over a wide range of input clock frequencies

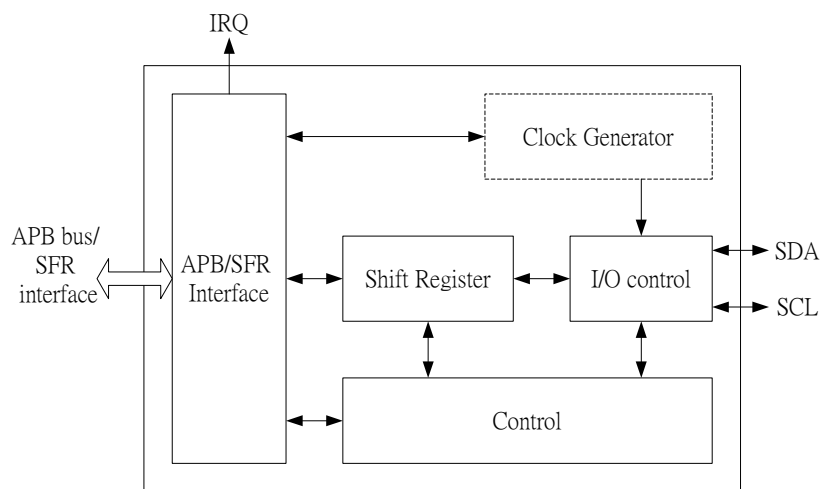
Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance among many devices.

The I²C Master/Slave core is a synthesizable soft IP core that connects to AMBA™ APB bus or the SFR interface of 8051μC for easy integration into SOC implementations. Both Normal mode (100Kbps) and Fast mode (400Kbps) are supported directly.

The I²C core performs a byte oriented data transport. Clock generation, address recognition and clock synchronization are all hardware controlled. Only simple software control is needed to handle the I²C transfer.

Block Diagram



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Description

The I²C Master/Slave Core is an AMBA compliant SOC peripheral. It can also be used as an SFR peripheral of a 8051 μ C. It is a slave module when connected to an AMBA system.

The I²C core provides the fast-mode, which allows the bit rate up to 400Kbps. Nevertheless it is downward compatible, i.e., it can be used in a 0 to 100 Kbps I²C bus system. The I²C-bus is a simple bi-directional 2-wire bus for efficient inter-IC data exchange. Features of the I²C-bus are:

- Only two bus lines are required: a serial clock line (SCL) and a serial data line (SDA)
- Each device connected to the bus is software addressable by a unique address
- Serial clock synchronization allows devices with different bit rates to communicate via the same serial bus

The I²C core performs a byte oriented data transport. Clock generation, address recognition and clock synchronization are all hardware Controlled. The I²C core logic handles byte transfer autonomously. Via two pins the external I²C-bus is interface to the I²C core. It only needs some simple software control flow to handle the I²C transfer. The I²C core can be connected to the APB bus of an AMBA system or the SFR interface of 8051 μ C for easy integration into SOC implementations.

Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User's Manual, Integration Guide, Verification Guide, and Test Guide

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