

UAPC-5100 DMA Controller

Features

- ◆ Comply with the *AMBA™ Spec. 2.0*
- ◆ 2 (8/4/2 configurable) DMA channels
- ◆ 4 (32/16/8/4 configurable) DMA requests
- ◆ Each channel has a 4-word (16/8/4/2 configurable) FIFO
- ◆ Single DMA and burst DMA request signals
- ◆ Supports memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transactions
- ◆ One AHB bus master for transferring data
- ◆ Incrementing, non-incrementing, and wrap incrementing addressing modes for source and destination
- ◆ Programmable DMA burst size
- ◆ Supports 8, 16 and 32-bit wide transactions
- ◆ Separate and combined DMA error and count interrupt requests
- ◆ Interrupt masking
- ◆ Raw interrupt status
- ◆ Flow controller can be the DMA controller, source peripheral, or destination peripheral

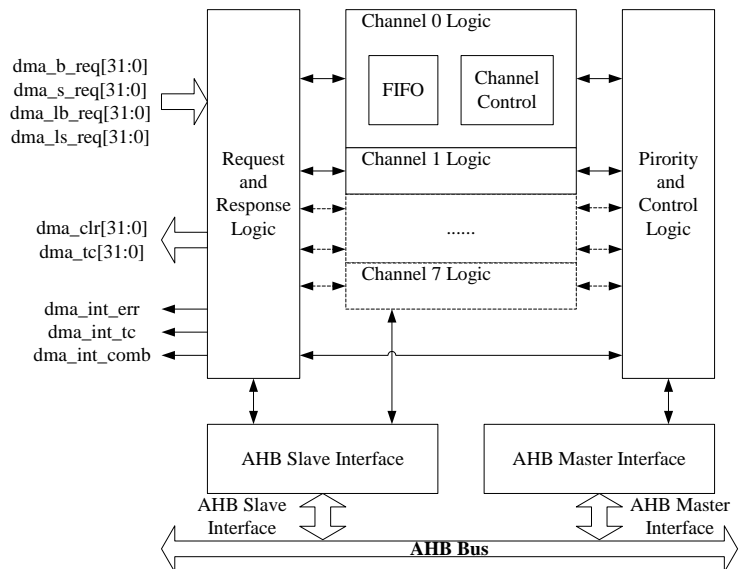
Overview

The DMA Controller is a synthesizable soft IP core connected to the AMBA™ AHB bus for easy integration into SOC implementations.

The DMA Controller provides 2 (8/4/2 configurable) DMA channels and 4 (32/16/8/4) DMA requests. Each DMA channel has a 4-word (16/8/4/2 configurable) FIFO. It has an AHB bus slave for programming the registers and AHB bus master for transferring data. It also supports the AHB burst transfers for a better performance.

The DMA Controller allows peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. The flow controller can be the DMA Controller, source peripheral, or destination peripheral.

Block Diagram



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Description

The DMA Controller is an AMBA™ compliant SOC peripheral. It has an AHB bus slave for programming the registers of the DMA Controller, and AHB bus master for transferring data. The DMA Controller supports the AHB burst transfers for a better performance. The operating frequency is 100MHz DC. The gate count is 10.8K for 2 channels, 4 requests, 4-word FIFO per channel, and 48.9K for 8 channels, 32 requests, 4-word per channel at TSMC 0.25µm process.

The DMA Controller provides 2 (8/4/2 configurable) DMA channels and 4 (32/16/8/4) DMA requests. Each DMA channel has a 4-word (16/8/4/2 configurable) FIFO. It supports incrementing, non-incrementing, and wrap-incrementing addressing modes for a source and destination, and also supports 8, 16 and 32-bit wide transactions. It provides flexible interrupt requests including interrupt masking and raw interrupt status.

The DMA Controller enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. The source and destination can each be either a memory region or a peripheral, and can be accessed through the AHB master. The flow controller can be the DMA Controller, source peripheral, or destination peripheral.

Deliverables

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive documents including Datasheet, User's Manual, Verification Guide, and Test Guide

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