

## UAPC-5400 Static Memory Controller

### Features

- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Independent configuration for up to eight memory banks, each up to 64MB
- ◆ Support static memory - mapped devices including RAM, ROM, flash, and burst ROM
- ◆ AHB burst transfers
- ◆ 8, 16, 32-bit wide external memory data bus
- ◆ Programmable wait states, bus turnaround cycles, output enable and write enable delays
- ◆ Independent byte lane control for each memory bank
- ◆ Use external control pins to configure size at reset for boot memory bank

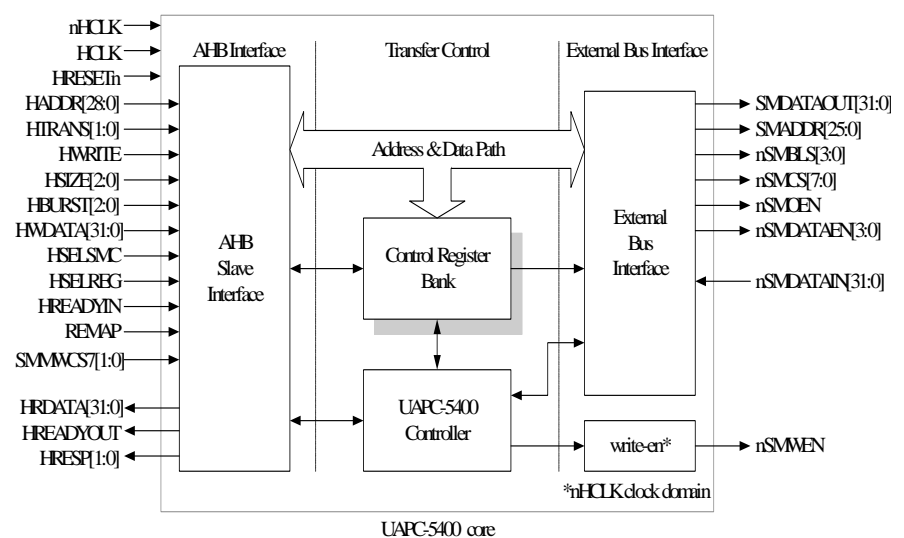
### Overview

The UAPC-5400 core is a synthesizable soft IP core that connected to AMBA™ AHB bus for easy integration into SOC implementations.

The UAPC-5400 supports up to eight independently configurable memory banks simultaneously. Each memory bank is capable of supporting: SRAM (synchronous or asynchronous), ROM, flash EPROM and burst ROM memory. Each memory bank can be configured to use 8, 16, or 32-bit wide external memory data bus.

This module also supports a simple request and grant protocol to share the external address and data buses with additional memory controller. It can be configured to allow boot ROM to be available instead of RAM at the base memory location immediately after reset, and the boot ROM device size can be configured at reset.

### Block Diagram



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## **Description**

The UAPC-5400 is an AMBA™ compliant SOC peripheral. It is a slave module that connects to the AHB bus and supports all of AHB burst transfers.

It supports up to eight independently configurable memory banks and each bank size up to 64MB. Each memory bank is capable of supporting: synchronous or asynchronous SRAM, ROM, flash EPROM, burst ROM and asynchronous page mode read operation devices. Each memory bank can be configured to use 8, 16, or 32-bit wide external memory data paths. Besides, the following parameters are programmable for each memory bank to meet various timing requirement of the memory device: write wait states for static RAM devices, read wait states for static ROM and RAM devices, initial and subsequent burst read WAIT state for burst ROM devices, bus turn-around cycles, output enable and write enable output delays, burst mode operation, write protection, chip select polarity and read byte lane enable control.

It also supports a simple request and grant protocol to share the external address and data buses with the additional memory controller through data bus interface. A simple address remap mechanism is provided that allows boot ROM to be available instead of RAM at the base memory location immediately after reset, and the boot ROM device size can be configured at reset.

## **Deliverables**

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

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