

## UAPC-5500 SDRAM Controller

### Features

- ◆ Compliance with AMBA™ Spec. 2.0
- ◆ Multiple AHB interfaces (up to 8 AHB slave ports) for accessing SDRAM
- ◆ Supports all AHB burst types
- ◆ Supports byte, half-word, and word accesses
- ◆ Supports busy and early terminations
- ◆ Supports 16Mb (2 bank), 64Mb, 128Mb, 256Mb, and 512Mb (4 bank) SDRAM
- ◆ Programmable SDRAM timing parameters – tRAS, tRCD, tRP, tWR, tRCAR, tMRD, tXSR, and tRC – can be programmed to timing values supported by different SDRAM vendors
- ◆ Supports auto-refresh mode with programmable refresh intervals
- ◆ Supports self-refresh and power-down modes
- ◆ Configurable FIFO depth
- ◆ Only supports Little-endian
- ◆ Does not generate split, retry, or error responses
- ◆ Only supports 16-bit-wide SDRAM

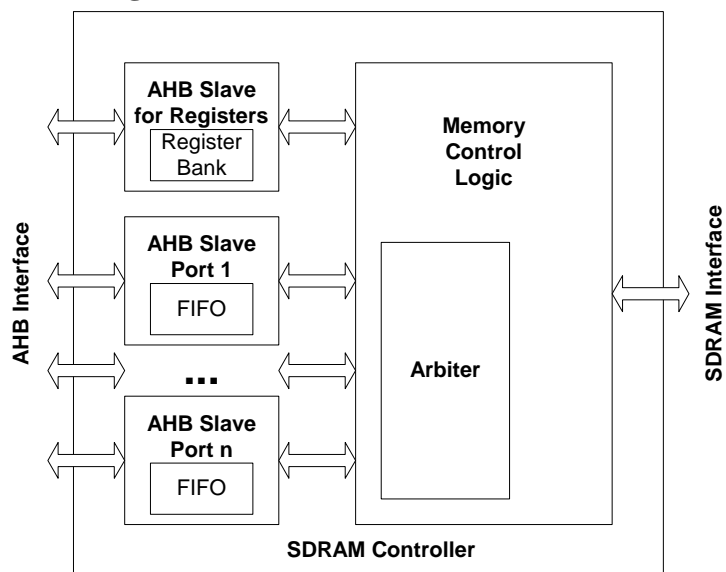
### Overview

The UAPC-5500 SDRAM Controller is a synthesizable soft IP core that can be connected to the AMBA™ AHB bus for easy integration into System-on-Chip (SOC) implementations.

UAPC-5500 provides multiple AHB interfaces (up to 8 AHB slave ports) to connect with a multi-layer AMBA system. It has an AHB slave for programming the registers, and other slaves for access memory. Each AHB slave port has a 4-word (32/16/8/4/2 configurable) FIFO. It supports all AHB burst transfer types, and byte, half-word, and word accesses.

The UAPC-5500 SDRAM Controller supports most SDRAM devices, which are of the 16-bit data width, and it can be programmed to meet different SDRAM timing specifications. It supports auto-refresh mode with programmable refresh intervals. It also supports self-refresh and power-down modes.

### Block Diagram



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## **Description**

The UAPC-5500 SDRAM Controller is an AMBA™ compliant System-On-Chip (SOC) peripheral. An AHB slave, UAPC-5500 is used for SDRAM data access. It can generate most of the commands to access an SDRAM device. The operating frequency ranges from Direct Current (DC) to 100MHz voltage. The gate count is 26.46K for 4 ports. For a typical 0.25µm process, there is one configurable 4-word FIFO per AHB port. When an additional AHB slave port is added, the gate count will increase by about 5.17K.

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## **Deliverables**

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set which includes Datasheet, User's Manual, Verification Guide, and Integration Guide

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