

## UAPC-5600 Local Memory Controller

### Features

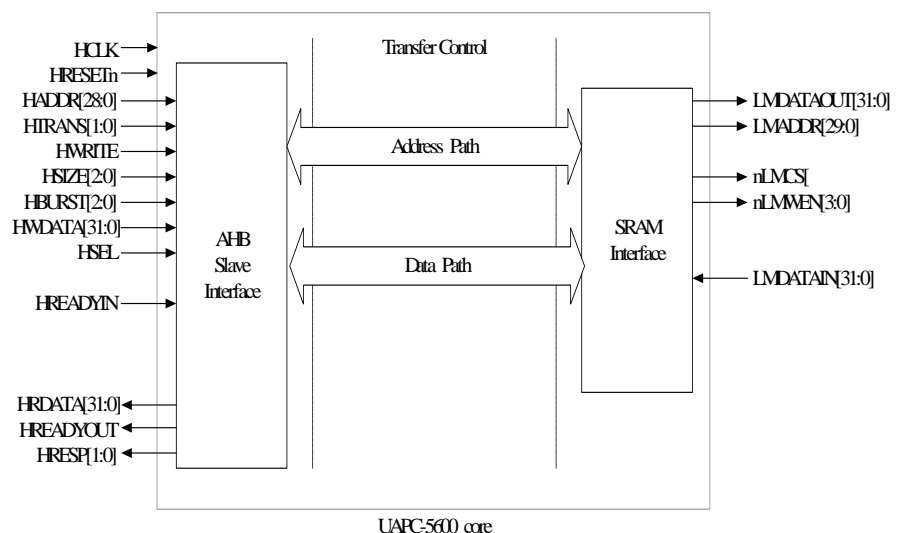
- ◆ Compliance with the AMBA™ Spec. 2.0
- ◆ Support embedded synchronous RAM read/write operation.
- ◆ 8, 16, 32-bit wide SRAM data bus
- ◆ Provide zero-wait speed sequential data transfer rate.

### Overview

The UAPC-5600 core is a synthesizable soft IP core that provides embedded synchronous RAM connected to AMBA™ AHB bus for easy integration into SOC implementations.

The UAPC-5600 supports Byte (8 bits), Halfword (16 bits) and Word (32 bits) transfer data bus size. It provides zero wait speed to read or write Embedded SRAM data sequentially.

### Block Diagram



### Global Unichip Corp.

TEL: +886-3-5646600      <http://www.globalunichip.com>  
 FAX: +886-3-5646000      e-mail: [info@globalunichip.com](mailto:info@globalunichip.com)  
 No. 10, Li-Hsin 6th Rd., Hsinchu Science Park, Hsinchu 300, Taiwan

## **Description**

The UAPC-5600 is an AMBA™ compliant SOC peripheral. It is a slave module that connects to the AHB bus and supports all of AHB burst and data size transfers.

It converts the AHB protocol to access SRAM data directly. This module provides full speed sequential data transfer rate to make high performance and high efficient AHB environment.

It can connect with four 8 bits data wide Embedded SRAM banks to supports Byte (8 bits), Halfword (16 bits) and Word (32 bits) transfer data bus size. Each SRAM bank size can be configured up to 1G(Byte).

## **Deliverables**

- Verilog RTL code
- Verification suite
- Synthesis script for Synopsys Design Compiler, Power Compiler and DFT Compiler
- Comprehensive document set including Datasheet, User Manual, Verification Guide, and Test Guide

### ***Global Unichip Corp.***

TEL: +886-3-5646600      <http://www.globalunichip.com>  
FAX: +886-3-5646000      e-mail: [info@globalunichip.com](mailto:info@globalunichip.com)  
No. 10, Li-Hsin 6th Rd., Hsinchu Science Park, Hsinchu 300, Taiwan