

UINF-0001 AHB USB1.1 Host Controller

Features

- ◆ Complies with USB Specification Rev 2.0
- ◆ Complies with AMBA Specification Rsion2.0
- ◆ Adapted from Universal Host Controller Interface Design Guide Rev1.1
- ◆ Supports data transfer at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
- ◆ Supports all four types of USB transfers: control, bulk, interrupt and isochronous
- ◆ Includes a RootHub with multi-port architecture
- ◆ Supports both of master and slave agents on AHB interface
- ◆ Directly addressable memory architecture; memory can be updated on-the-fly
- ◆ Supports Synchronization Circuit between USB clock and AHB clock (No Extra synchronization circuit is needed)
- ◆ Supports USB Host Controller I/O registers for software communication channel
- ◆ Re-uses Linux or WinCE UHCI Host Controller driver with minor change on register offset
- ◆ Supports uP interrupt request interface

Overview

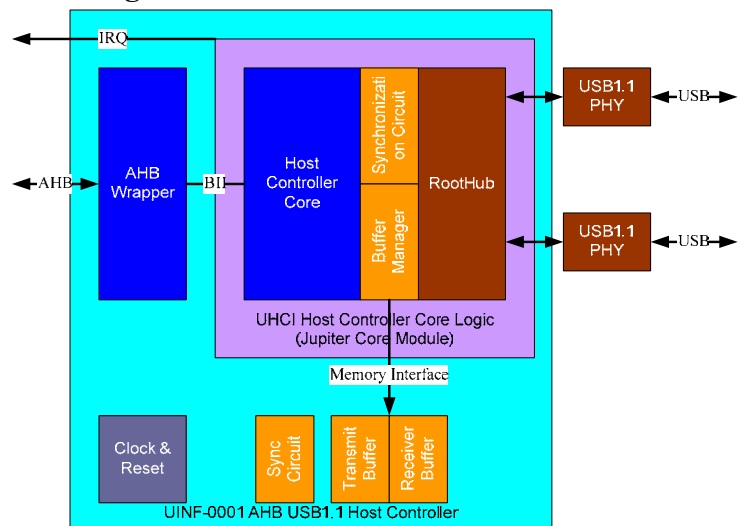
UINF-0001 is adapted from UHCI Design Guide Rev1.1 and only USB Host Controller I/O registers are implemented. For the PCI

Configuration Registers, they are enumerated by software system. A RootHub is embedded in UINF-0001, by default, two downstream ports are implemented. For more downstream ports, a minor modification is required.

An unlimited synchronization circuit is embedded in UINF-0001, user can use this IP in any system clock rate without AHB-to-AHB bridge or other logic module for synchronization issue.

A digital PLL logic circuit is implemented and meets the requirement of USB2.0 specification. Only a USB1.1 transceiver IO pad is expected on chip integration. The interface also meets the definition of PDIUSBP11A. That would easy user on FPGA verification.

Block Diagram



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Description

UINF-0001 AHB USB1.1 Host Controller is designed for embedded system using. AMBA2.0 AHB bus is expected as default backbone. User can modify the wrapper for adapting different system bus. The function of UINF-0001 is fully verified under GUC's GPrime platform with Linux OS 2.4.

Deliverables

- **One-Page Summary**
- **Datasheet**
- **User's Manual**
- **Verification Guide**
- **Integration Guide**
- **Installation Guide**
- **Synthesizable RTL**
- **Synopsys Scripts**
- **Regression List**
- **Function Verification Model**

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