

UINF-0201 AHB Ethernet 10/100Mbps MAC

Features

- ◆ Comply with AMBA specification 2.0
- ◆ AHB bus with Master and Slave mode
- ◆ AHB with programmable bust size
- ◆ Serial ROM interface support
- ◆ PHY management interface MDIO support
- ◆ Comply with IEEE 802.3u MII interface
- ◆ Full /Half Duplex capability
- ◆ Support IEEE 802.3x Full Duplex Flow

Control

- ◆ Support IEEE 802.1Q VLAN mode
- ◆ Support Loopback test mode
- ◆ Includes two DMA to reduce CPU loading
- ◆ Independent TX and RX FIFO
- ◆ Configurable FIFO size (128B~2KB)
- ◆ Embedded Memory BIST block

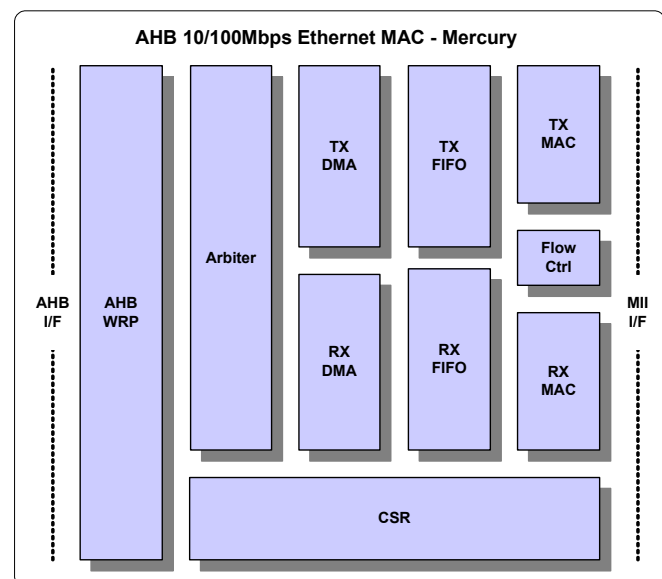
Overview

The Mercury is a 10/100Mbps AHB Ethernet MAC. It includes AHB wrapper, DMA engine, on-chip memory (TX/RX FIFO), TX MAC, RX MAC and MII interface.

The DMA handles the data transfer between system memory and on-chip memory. With DMA engine, it will reduce CPU loading and enhance Mercury performance. An industry-standard interface is necessary for reusable reason. The Mercury is fully compliant with AMBA 2.0 and IEEE802.3u Standard. An AHB wrapper in Mercury provides the transfer between GUC internal interface, BII (Bus Independent Interface) and AHB interface.

The memory size always dominates the hardware cost. For this reason, the FIFO size in Mercury is configurable (128-Byte ~ 2K-Byte), dependent on user's application or system bus performance.

Block Diagram



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Description

Mercury includes following 10 subblocks:

TxMAC (Transmit Media Access Control) – Move the data from the internal TX FIFO and encapsulate the frame, then move the data to PHY layer

RxMAC (Receive Media Access Control) – Receive the frame from PHY layer and filter the date, then move the data to internal RX FIFO.

TxDMA (Transmit Direct Memory Access) –After host processor has prepared transmit buffer, it notify TxDMA to take it. The TxDMA will move data from host memory to TX FIFO.

RxDMA (Receive Direct Memory Access) – Move the data from RX FIFO to host memory. When a frame has received, Mercury will start to move data if host memory has prepared by host processor.

TX FIFO (Transmit FIFO) – 128 Byte ~ 2K Byte two port register file that buffer the data from host memory before move to PHY layer.

RX FIFO (Receive FIFO) – 128 Byte ~ 2K Byte two port register file that buffer the data from PHY layer before move to host memory

CSR (Control and Status Registers) – The CSRs are accessed by software driver and are used for initialization, pointers, commands, and status report. The CSRs are quad-word aligned (4bytes), and the host processor uses a single instruction to access CSRs.

AHB WRP (Advanced High-performance Bus Wrapper) – This block translates the signals between BII I/F to AHB I/F, and there are master and slave mode in AHB wrapper.

Arbiter – This block decide which master (TX DMA or RX DMA) can access AHB bus.

Flow CTRL (Flow Control) - The flow control recognizes MAC control frame for full-duplex links. This block also generates pause frames to avoid data overflow.

Deliverables

A. Documentation

- ◆ One page summary
- ◆ Data Sheet
- ◆ User's manual
- ◆ Integration guide
- ◆ Installation guide

B. Logic/SW Design

- ◆ Synthesizable RTL
- ◆ Regression list
- ◆ Synthesis scripts
- ◆ Linux 2.6 driver

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