

## UINF-0301 AHB IDE Host Controller

### IDE Features

- ◆ Two clock domain between AHB and ATA interface.
- ◆ Compliant with AT/ATAPI-6 interface.
- ◆ Don't support Queued and Overlapped command.
- ◆ Support programmable IO modes 0-4.
- ◆ Support Multi-word DMA modes 0-2.
- ◆ Support Ultra DMA modes 0-5.
- ◆ ATA Interrupt Support.
- ◆ Configurable timing control for running at different clock frequency.
- ◆ Doesn't support Queue command feature set and Overlapped command set.

### AHB Features

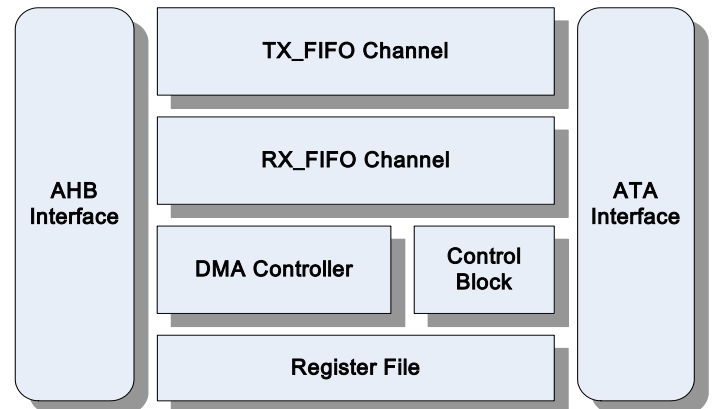
- ◆ Compliant with AMBA Specification Revision 2.0.
- ◆ Support little endian AHB bus with 32 bits data bus transaction.
- ◆ Support byte, half-word, word transactions.
- ◆ AHB slave interface doesn't support split and locked transactions.

### DMA Features

- ◆ Passive Descriptor-Based DMA engine to transfer block of data.
- ◆ DMA has AHB and IDE Master agent to transfer data.
- ◆ Each direction has 128 bytes FIFO to

buffering data.

### Block Diagram



The Atlas IDE host controller offers basic ATA/ATAPI-6 command sets to access IDE devices. User can dynamic adjusts IDE transfer mode through AHB register setting. And for improving IDE transfer performance, user can base on actually system frequency to set Atlas timing parameters.

Two FIFO channel and DMA controller are responsible for the DMA data transfer, and Register File and Control Block provides the operating registers and control signals of Atlas.

For block data transfer Atlas provides a Descriptor-Based DMA to transfer data from/to IDE devices without consuming CPU resource.

### *Global Unichip Corp.*

TEL: +886-3-5646600

<http://www.globalunichip.com>

FAX: +886-3-5646000

e-mail: [info@globalunichip.com](mailto:info@globalunichip.com)

No. 10, Li-Hsin 6th Rd., Hsinchu Science Park, Hsinchu City, 300, Taiwan

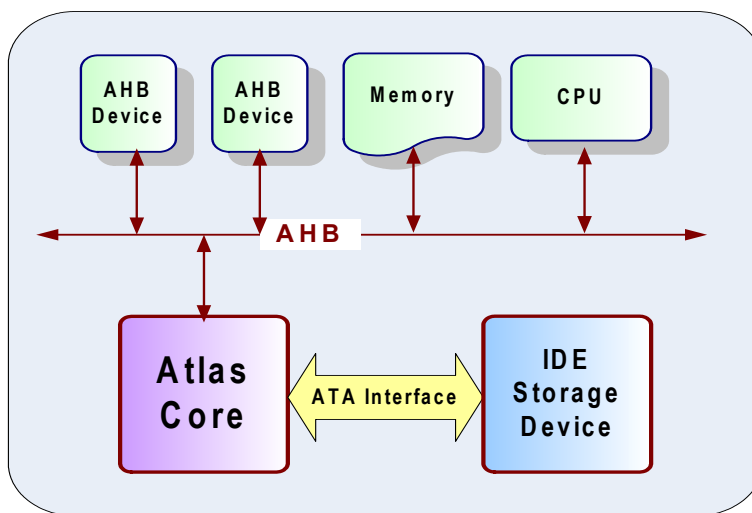
Copyright © 2005 Global Unichip Corp. All Rights Reserved

## Description

The AHB IDE host controller core provides efficient and easy-to-use interface to transfers data from/to host system to/from ATA compatible IDE storage devices, and supports up to 2 IDE devices, device0 and device1. It implements the programmable IO modes 0-4, Multi-word DMA modes 0-2, and Ultra DMA modes 0-5. For easy integration, the Atlas is designed to interface to host system by high performance AHB bus interface.

It also provides configurable timing control for any timing mode of PIO mode, Multi-word DMA mode, and Ultra DMA mode transfers while running at any clock frequency.

The AHB IDE host controller core has been verified on GUC GPrime platform.



## Deliverables

- One page summary
- Datasheet
- User's manual
- Verification guide
- Verification Plan
- Integration guide
- Synthesizable Verilog RTL files
- Synthesis scripts file
- Regression testbench
- Function verification model

## ***Global Unichip Corp.***

TEL: +886-3-5646600

<http://www.globalunichip.com>

FAX: +886-3-5646000

e-mail: [info@globalunichip.com](mailto:info@globalunichip.com)

No. 10, Li-Hsin 6th Rd., Hsinchu Science Park, Hsinchu City, 300, Taiwan

Copyright © 2005 Global Unichip Corp. All Rights Reserved