

ULVDS-3860-250EF

0.25mm EmFlash 3.3V LVDS Receiver 24-bit FPD Link

Features

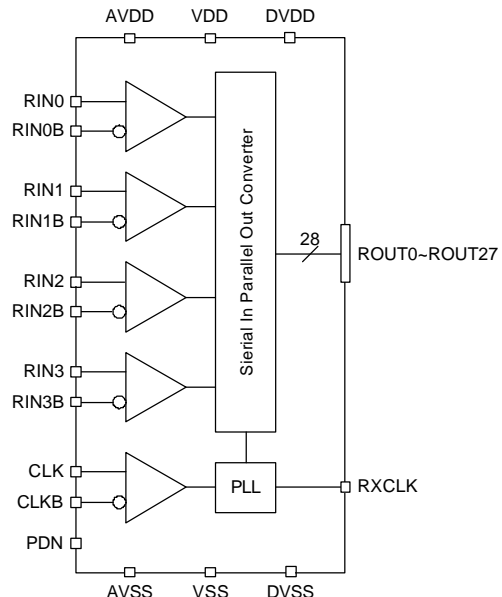
- ◆ TSMC 0.25um split gate Emflash 2P5M Salicide 2.5V/3.3V CMOS process with 1P4M layout
- ◆ 2.5V and 3.3V $\pm 10\%$ supply operation
- ◆ 2.5V digital output signal
- ◆ 20 to 110 MHz shift clock support
- ◆ 4:28 data channel expansion at up to 385 Megabytes/sec bandwidth
- ◆ Falling-edge clock triggered outputs
- ◆ Supports VGA, SVGA, XGA and Single Pixel SXGA
- ◆ PLL requires no external components
- ◆ Support floating and terminated input fail-safe
- ◆ Power-down capability
- ◆ Compatible with TIA/EIA-644 LVDS standard
- ◆ Compatible with the National DS90CF386, Thine THC63LVDF84B

Overview

The ULVDS-3860-250EF FPD-link receiver converts the four LVDS (Low Voltage Differential Signaling) data streams back into parallel 28bits of 2.5V CMOS data. The receiver's outputs are falling edge strobe.

The ULVDS-3860-250EF requires only five line-termination resistors for the differential inputs. An active-low power down input can be used to inhibit the clock and shut off the LVDS receivers for lower power consumption.

Block Diagram



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Description

The ULVDS-3860-250EF is an FPD-link LVDS receiver specifically designed to support data receiving from graphics controller to LCD panels. It converts the four LVDS data streams that transmit from graphics controller back into 28-bits of CMOS data. At a transmit clock frequency of 110MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (Hsync, Vsync, DE and CNTL) are transmitted at a throughput of 3.08 Gbps.

The ULVDS-3860-250EF is designed in TSMC 0.25um split gate Embflash 2P5M Salicide 2.5V/3.3V CMOS process with 1P4M layout. The test chip is available in a 64-lead LQFP package. The evaluation board is available with the test chip.

Deliverables

- ◆ **Comprehensive document set**
- ◆ **Hard macro**
- ◆ **Synopsys™ synthesis model**
- ◆ **Verilog model**
- ◆ **TLF model**
- ◆ **LEF model**
- ◆ **Test chip**
- ◆ **Evaluation board**

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