

ULVR-3318-180 0.18 μ m 3.3V to 1.8V 50mA Linear Voltage Regulator

Features

- ◆ 0.18 μ m 1.8V/3.3V logic salicide CMOS process with 1P4M layout
- ◆ 3.3V to 1.8V conversion
- ◆ Maximum output load current: 50mA
- ◆ Operation temperature range:-25 $^{\circ}$ C~125 $^{\circ}$ C
- ◆ Build-in voltage reference
- ◆ Power down mode available
- ◆ Stable with >1 μ F ceramic capacitor
- ◆ Customized 50mA output current extension module is available
- ◆ Cell size : 250 μ m x 270 μ m

Applications

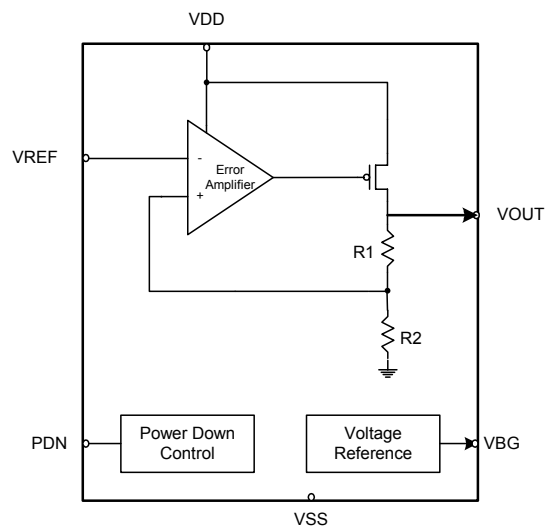
- PCMCIA Card
- Digital Camera
- Battery Powered Application
- Mobil phone
- MP3 player

Overview

ULVR-3318-180 is a linear voltage regulator IP (LVR) for powering the 1.8V digital core circuit from single 3.3V supply voltage. The regulator incorporates a bandgap voltage reference circuit for fixing reference voltage generation. The feedback loop sets the output voltage to 1.8V with small voltage coefficient regardless whether the output load current changes from 0mA up to 50mA or the supply voltage varies.

A bypass capacitor is required for proper frequency compensation. A power down mode is available for the regulator.

Block Diagram



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Description

The output voltage of the regulator (VOUT) is set by the VREF. The relationship between the regulator output VOUT and input reference voltage VREF is defined as :

$$V_{out} = V_{ref} \times 1.48 \quad (1.12V \leq V_{ref} \leq 1.30V)$$

A customized current extension module, ULVR-3318-180-EX is available for output current extensions. Each current extension module applies up to 50mA output current with 1.8V output voltage. By using ULVR-3318-180 incorporation with ULVR-3318-180-EXs can extend the output current to 100mA or 150mA base on the numbers of current extension modules without multiple the overall sizes.

The ULVR-3318-180 is fabricated in TSMC 1P6M 0.18um 1.8V/3.3V logic salicide CMOS process with 1P4M layout. The test chip of ULVR-3318-180 is available in a 64-lead LQFP package. An evaluation board is also available.

Deliverables

- Comprehensive document set
- Hard macro
- Synopsys™ synthesis model
- Verilog model
- TLF model
- LEF model
- Testchip and evaluation board

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