



ARM926EJ

Features

- ◆ Selectable size instruction and data caches
- ◆ 32/16-bit RISC architecture (ARMv5TEJ)
- ◆ 32-bit ARM instruction set for maximum performance and flexibility
- ◆ 16-bit Thumb instruction set for increased code density
- ◆ DSP instruction extensions and single cycle MAC
- ◆ ARM Jazelle technology
- ◆ MMU which supports operating systems including Symbian OS, Windows CE, Linux
- ◆ Flexible instruction and data cache sizes
- ◆ Instruction and data TCM interfaces with wait state support
- ◆ EmbeddedICE-RT logic for real-time debug
- ◆ Industry standard AMBA bus AHB interfaces
- ◆ ETM interface for Real-time trace capability with ETM9
- ◆ Optional MOVE Coprocessor delivers video encoding performance

Overview

The ARM926EJ-S is a member of ARM9 family of general-purpose microprocessors. The ARM926EJ includes features of selectable instruction and data cache sizes, Java bytecode execution, 16-bit Thumb instruction set, tightly coupled memory (TCM) interfaces, memory management unit (MMU), DSP extensions, embedded trace macrocell (ETM) interface and dual AHB bus interface. It is targeted at multi-tasking applications.

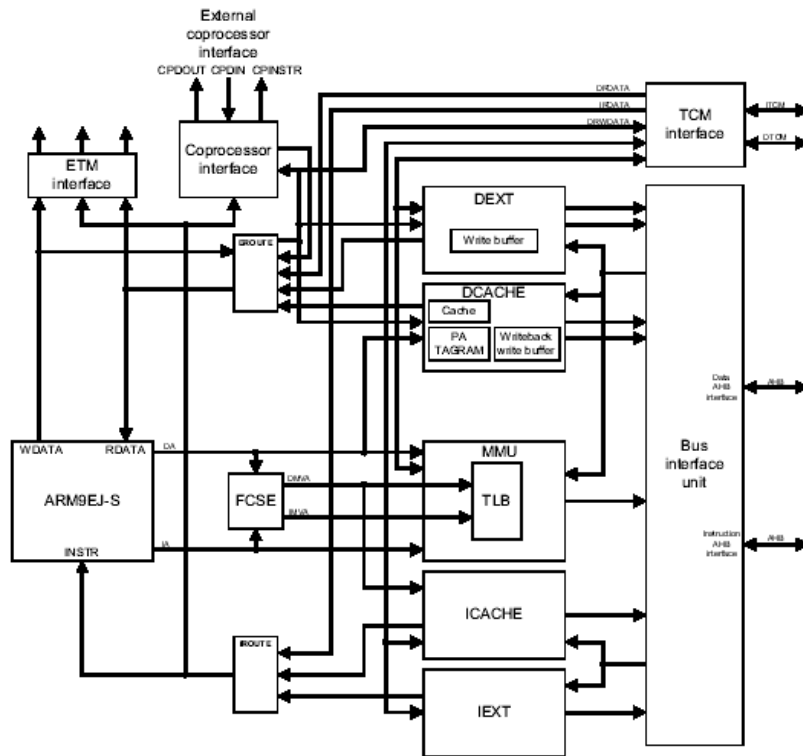
Deliverables

- ARM9E Technical Reference Manual
- ARM926EJ Technical Reference Manual
- ARM926EJ Errata List
- ARM926EJ-S Core Design Simulation Models
- ARM926EJ TSMC Static Timing View - Synopsys .lib
- ARM926EJ TSMC Static Timing View - Synopsys .CLF
- ARM926EJ Configuration & Performance Summary – PDF
- ARM926EJ I/O Port (Stub) View – Verilog

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Block Diagram



Description

The ARM926EJ-S macrocell is fully synthesizable, and features a Jazelle technology enhanced 32-bit RISC CPU, flexible size instruction and data caches, tightly coupled memory (TCM) interfaces, memory management unit (MMU). It also provides separate instruction and data AMBA bus compliant AHB interfaces particularly suitable for Multi-layer AHB based systems. The ARM926EJ-S core implements the ARMv5TEJ instruction set and includes an enhanced 16 x 32-bit multiplier, capable of single cycle MAC operations. The ARMv5TEJ instruction set includes 16-bit fixed point DSP instructions to enhance performance of many signal processing algorithms and applications as well as supporting Thumb and Java bytecode execution.

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