

UPLL-1001-130 0.13um 1.2v/3.3v PLL for Audio Application

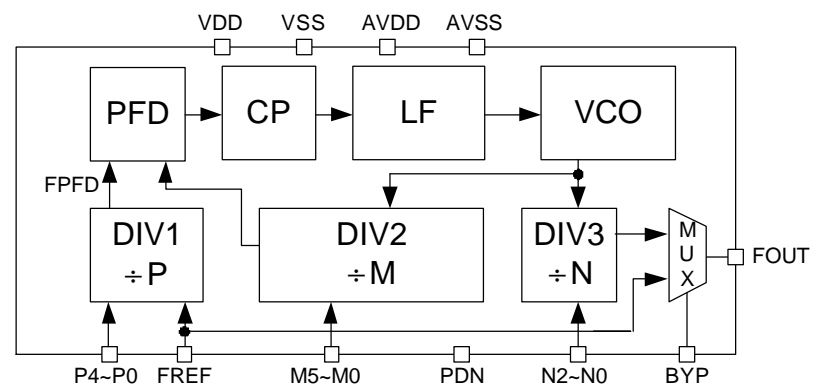
Features

- ◆ 0.13um 1P8M 1.2v/3.3v logic salicide CMOS process with 1P4M layout
- ◆ Separated analog and digital power/ground
- ◆ Fully integrated PLL-based audio clock generator with built-in loop filter
- ◆ Bypass mode
- ◆ Power down mode
- ◆ Small area size

Overview

The UPLL-1001-130 is a PLL-based clock generator for audio application. It integrates a voltage-controlled oscillator, a phase frequency detector, a charge pump, a loop filter and two frequency dividers. It can generate frequency range for general digital audio frequency with a 6-bit main frequency divider, a 5-bit pre-divider and a 3-bit post divider. The supported sampling clock rates are 8Khz, 16Khz, 24Khz, 32Khz, 44.1Khz, 48Khz, and 96Khz. The UPLL-1001-130 is designed with TSMC 0.13um 1P8M 1.2v/3.3v logic salicide CMOS process.

Block Diagram



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Description

The circuit of UPLL-1001-130 is a PLL designed for audio clock generation. The output frequency of the PLL can be programmed by the inputs (P4~P0, M5~M0, N2~N0). The following table is the typical frequency settings for digital audio application. Output frequency of FOUT is 128x, 256x, 384x or 512x of the target audio clock rate.

Deliverables

- ◆ **Comprehensive document set**
- ◆ **Hard macro**
- ◆ **Synopsys™ synthesis model**
- ◆ **Verilog model**
- ◆ **TLF model**
- ◆ **LEF model**
- ◆ **Test chip and evaluation board**

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