

UPLL-1002-180 0.18um 1.8V 80MHz~500MHz Frequency

Synthesizer (PLL)

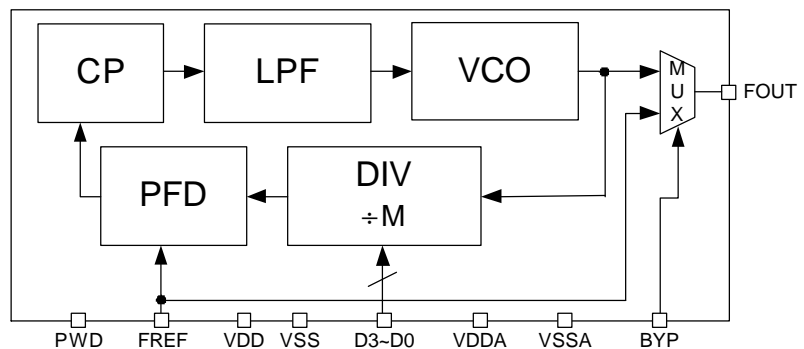
Features

- ◆ 0.18um 1P6M 1.8v/3.3v logic salicide CMOS process with 1P3M layout
- ◆ Separated analog and digital power/ground
- ◆ Fully integrated PLL-based clock generator with built-in loop filter
- ◆ Wide output frequency rang (FOUT: 80MHz ~ 500MHz)
- ◆ Flexible input frequency range (20MHz ~ 125MHz)
- ◆ A programmable frequency divider (4-bits main divider)
- ◆ Low jitter
- ◆ Bypass mode
- ◆ Power down mode

Overview

The UPLL-1002-180 is a PLL-based clock generator with built-in loop filter. It integrates a voltage-controlled oscillator, a phase frequency detector, a charge pump, a loop filter and two frequency dividers. It can generate frequency range within 80MHz~500MHz with a 4-bit main frequency divider. The UPLL-1002-180 is designed with tsmc 0.18um 1P6M 1.8v/3.3v logic salicide CMOS process.

Block Diagram



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Description

The circuit of UPLL-1002-180 is a PLL designed for clock generation. The output frequency of the PLL can be programmed by the inputs D3~D0. The frequencies are defined as follows:

$$F_{OUT} = F_{REF} * M \quad (16 \geq M \geq 2, F_{REF} \geq 20Mhz, 500Mhz \geq F_{OUT} \geq 80Mhz)$$

The value of D3~D0 is encoded with unsigned binary code. M is the value of [D3:D0].

Deliverables

- ◆ Comprehensive document set
- ◆ Hard macro
- ◆ Synopsys™ synthesis model
- ◆ Verilog model
- ◆ TLF model
- ◆ LEF model
- ◆ Test chip and evaluation board

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