

UPOR-2502-250 0.25mm 2.5V Power On Reset Circuit

Features

- ◆ No external components required
- ◆ Embedded Schmitt Trigger for supply noise rejection
- ◆ Negative logic reset signal (Low active reset)
- ◆ Single Supply +2.5V
- ◆ Low quiescent current (Typical < 1uA) after Reset
- ◆ Testchip available in SOP-16 Package
- ◆ Power slew (slow ramp) detection

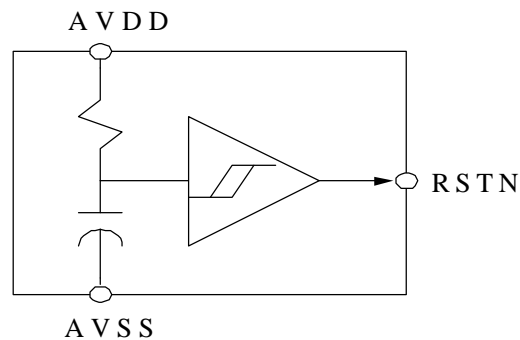
Applications

- ◆ Microprocessor reset
- ◆ Sequential circuit resets
- ◆ Power-up delay

Overview

UPOR-2502-250 is a power on reset circuit (POR) designed for finite-state-machine or microprocessor-based design. The circuit monitors the supply-voltage and provides the reset signal to the digital core after power-up. The internal delay network provides a fixed but inaccurate delay time to prevent power dangling.

Block Diagram



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Description

The UPOR-2502-250 is a simple power-on reset circuit features internal RC delay network and Schmitt trigger. While the power power-up, the output signal RSTN is at logic "0" initially. After a certain amount of delay time, the reset signal RSTN goes to and remains logic "1". There is no power dissipation after RSTN goes to logic "1".

The UPOR-2502-250 is fabricated in TSMC 1P3M 0.25 μ m 2.5V salicide CMOS logic process. The UPOR-2502-250 test chip is available in a 16-lead SO package. There is an evaluation board available with the test chip.

Deliverables

- ◆ Hard macro
- ◆ Synopsys™ synthesis model
- ◆ Verilog model
- ◆ Test chip
- ◆ Evaluation board

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