

GUC D2D IP Roadmap & Value Proposition

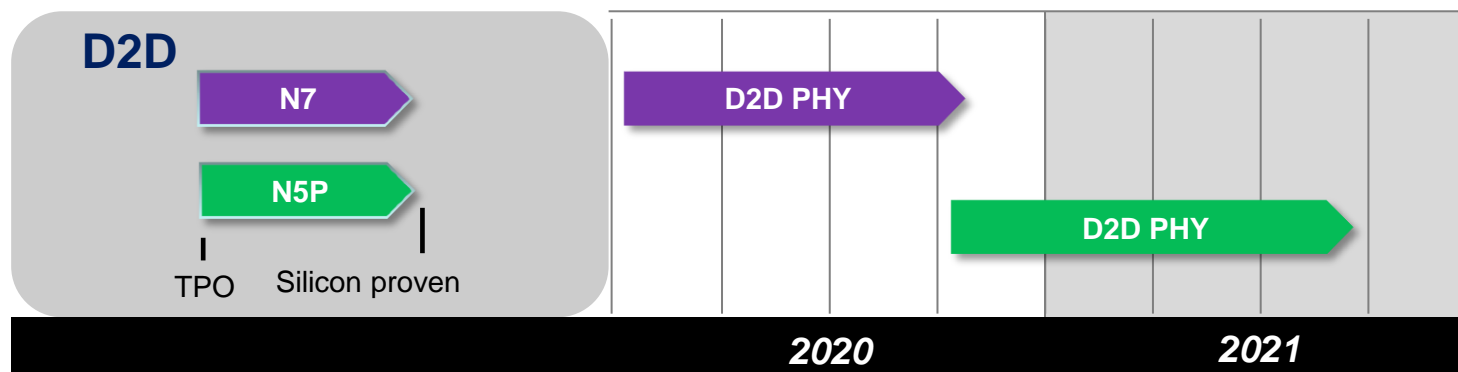
◆ The most optimized solution on power, area and speed for multi-die integration by InFO or CoWoS

- Power : below 0.25 pJ/bit (single 0.75V power supply required)
- Area : 0.7 Tbps/mm² (RX and TX)
- Beachfront : 0.7 Tbps/mm (RX and TX)
- Speed : 8 Gbps/lane
- Less substrate layers required

◆ Reliable Solution

- No BER, error correction is not used
- DFT functionality for separate dies testing and InFO/CoWoS assembly testing
- Redundant lanes embedded to achieve better yield

◆ GUC provides Total Service Package, including sub-system built, SI/PI/Thermal co-sim and sub-system bring-up services



GUC HBM IP Roadmap & Value Proposition

- ◆ **Silicon Proven 2.0G/2.4G HBM2 on N16/N7**
- ◆ **World First TPO 3.2G HBM2E on N7, Silicon available now**
 - Jan/2019 (one month after HBM2E standard released)
- ◆ **World Best Controller Performance**
 - > 90% bus utilization at random access (optimized for AI/HPC appl.)
- ◆ **PHY + Controller + CoWoS as Total Solution**
 - 4x HBM2, CoWoS assembly yield > 99% ; 6x HBM2E in early 2Q20
- ◆ **Fully Compliant with Vendor's HBM Memory**
- ◆ **GUC provides Total Service Package, including sub-system built, SI/PI/Thermal co-sim and sub-system bring-up services**

