GUC multi-die interLink (GLink) Value Proposition

◆ The most optimized solution on power, area and speed for multi-die integration by InFO or CoWoS
  - GLink-fs 1.0 key parameters
    - Power: below 0.256 pJ/bit (0.75V supply)
    - Area: 2Tbps/2.5mm² (RX and TX)
    - Beachfront: 2Tbps/3mm (RX and TX)
    - Speed: 8 Gbps/lane
    - Latency: 7.5~8.5ns
  - GLink-fs 2.0 key parameters
    - Power: below 0.25 pJ/bit (0.75V supply)
    - Area: 4Tbps/2.7mm² (RX and TX)
    - Beachfront: 4Tbps/3mm (RX and TX)
    - Speed: 16Gbps/lane
    - Latency: 7.5~8.5ns
    - Backward compatible to GLink-fs 1.0

◆ Reliable Solution
  - No BER, error correction is not used
  - DFT functionality for separate dies testing and InFO/CoWoS assembly testing
  - Redundant lanes embedded to achieve better yield

◆ GUC provides Total Service Package
  - sub-system built
  - InFO_RDL/Interposer design
  - SI/PI/Thermal co-sim services
GUC HBM IP Roadmap & Value Proposition

- **Production HBM2 2.0G**
- **World First N7 3.2G HBM2E Silicon Proven**
  - Demoed in TSMC OIP; Customer ASIC design in
- **World First N5 3.2G HBM2E T/Oed**
  - Adopted by leading customer
- **World Best Controller Performance**
  - > 90% bus utilization at random access (optimized for AI/HPC appl.)
- **PHY + Controller + CoWoS as Total Solution**
  - Total Service Package, including sub-system built, SI/PI/Thermal co-sim and subsystem bring-up services

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